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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,545	01/12/2004	Shinji Tojo	XA-9745A	9264

181 7590 08/08/2006

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
JEFFERSON, QUOVAUNDA	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,545	TOJO ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. 10/242,720.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objection

Claims 14-22 are objected to because the specification, while being enabling for "the pitch of plural salient electrodes is larger than the pitch of said leads at portions corresponding respectively to the plural salient electrodes", does not reasonably provide enablement for "the pitch of plural salient electrodes is smaller than the pitch of said leads at portions corresponding respectively to the plural salient electrodes". The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to the use of the invention commensurate in scope with these claims.

Applicant's specification clearly cites on page 4, line 19 the limitation "the pitch of plural salient electrodes is larger than the pitch of said leads at portions corresponding respectively to the plural salient electrodes". While later, the applicant does teach that the pitch of the lead changes due to thermal expansion, yet applicant never states in the specification that the pitch of the lead is at any point larger than the pitch of the electrode.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 14 of the present invention is generic with respect to the patented claim 12 of the US Patent No. 6,699,737. A species claim anticipates a generic claim; therefore, the patented claim anticipates the examined claim. See MPEP 806.04 (i).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 14-22 rejected under 35 U.S.C. 102(a) as being anticipated by Mita et al, US Patent Application Publication 2001/0002066.

Regarding claim 14, Mita teaches a method of manufacturing a semiconductor device, comprising the steps of (a) providing a semiconductor chip **1**, said semiconductor chip having a main surface and a plurality of salient electrodes **2** formed on said main surface (figure 6a and [0032]), (b) providing a wiring substrate **6**, said

wiring substrate having a thin film base **4** formed by an insulator and also having a plurality of leads **3** corresponding respectively to said plural salient electrodes of said semiconductor chip (figure 6 and [0033]), and (c) bonding said plural salient electrodes to said plural leads respectively [0076], wherein, in said wiring substrate provided in said step (b), the pitch of said plural salient electrodes is smaller than the pitch of said leads at the portions corresponding respectively to the plural salient electrodes (figures 4B and 5A), wherein said plural leads are fixed to said thin film base at their portions to be bonded to said salient electrodes, and wherein said step (c) includes a step of positioning said wiring substrate and said semiconductor chip to predetermined positions while from each other, a step of keeping the two spaced apart holding the portion of said wiring substrate located around an area where the bonding between said salient electrodes and said leads is performed (figures 6), grippingly by means of a jig **13**, while keeping the wiring substrate and the semiconductor chip spaced apart from each other (figure 6), and a step of pushing said wiring substrate by said jig to bring said leads into contact with said salient electrodes (figure 6).

Regarding claim 15, Mita further teaches wherein the bonding between said salient electrodes and said leads in said step (c) is performed by forming Au-Sn eutectic bond between the two [0004].

Regarding claim 16, Mita further teaches the bonding between said salient electrodes and said leads in said step (c) is performed by forming Au-Au bond between the two [0058-0064].

Regarding claim 17, Mita further teaches the bonding between said salient electrodes and said leads in said step (c) is performed at a temperature of not higher than the glass transition temperature of said insulator which constitutes said thin film base [0172].

Regarding claim 18, Mita further teaches said thin film base is flexible [0140].

Regarding claim 19, Mita further teaches the bonding between said salient electrodes and said leads in said step (c) is performed by bringing the salient electrodes and the leads into contact with each other while heating said semiconductor chip to a temperature higher than the temperature of said wiring substrate [0172].

Regarding claim 20, Mita further teaches the bonding between said salient electrodes and is performed by bringing the leads into contact with each said leads in said step (c) salient electrodes and the other while heating said semiconductor chip to a temperature higher than the temperature of said wiring substrate with use of a jig [0172, 0178].

Regarding claim 21, Mita further teaches heating said wherein the temperature of said jig for semiconductor chip is not lower than the glass transition temperature of said insulator, which constitutes said thin film base [0165].

Regarding claim 22, Mita further teaches the temperature of said wiring substrate before the contact between said salient electrodes and said leads is not higher than the glass transition temperature of said insulator which constitutes said thin film base [0172, 0178].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fernando Toledo
Patent Examiner
Art Unit 2823

QVJ